INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
YOR920000660U[redacted]13959)	09/855,240
Applicant(s)	
Louis L. Hsu, et al.	
Filing Date	**Group Art Unit**
May 15, 2001	2818

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

KMM		Yasuharu Sato, et al., "Fast Cycle RAM (FCRAM); a 20-ns Random Row Access, Pipe-Lined Operating DRAM", IEEE Symposium on VLSI Circuits Digest of Technical Papers, pp. 22-25, June 1998
KMM		Yasuhiro Agata, et al., "An 8ns Random Cycle Embedded RAM Macro with Dual-Port Interleaved DRAM Architecture (D2RAM), IEEE International Solid-State Circuits Conference, pp. 392-393, February 9, 2000

EXAMINER	DATE CONSIDERED
Kimberly M Lee-Mayo	12/2002

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.